UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/672,639 | 09/28/2000 | Gary Dan Dotson | 00AB154 | 7884 |

7590 06/01/2004

Allen-Bradley Company Inc
Attention: John J Horn
Patent Dept/704P Floor 8 T-29
1201 South Second Street
Milwaukee, WI 53204

| EXAMINER | |
|---|---|
| WANG, JIN CHENG | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2672 | 17 |

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Advisory Action | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/672,639 | DOTSON ET AL./ | |
| | Examiner | Art Unit | |
| | Jin-Cheng Wang | 2672 | |

*--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

THE REPLY FILED 19 May 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1-14 and 22-29*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)( PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

Continuation of 5. does NOT place the application in condition for allowance because:

1) Applicants argue in essence that neither Tjandrasuwita nor Reddy, et al. teach a single output that can provide data to both CRTs and LCDs as claimed. In response, the Examiner asserts that Reddy teaches the claim limitation of "a single output that can provide data to both CRTs and LCDs". It is clear from Fig. 1, 2 and 7 that data is provided from a single output from Look-up-Table 103 of Fig. 1, Fig. 2 to both CRTs and LCDs. Therefore, Reddy teaches the claim limitation. Moreover, Tjandrasuwita also suggests the claim limitation of "a single output that can provide data to both CRTs and LCDs" because Tjandrasuwita teaches in Fig. 1 a single output within the display graphics controller 107 with the same data being sent to the CRTs and LCDs.

2) Applicant argues that there is not proper motivation to combine Tjandrasuwita and Reddy, et al. at least because Reddy, et al. teaches away from a single output. In response, the Examiner asserts that Reddy teaches the claim limitation of "a single output" wherein the single output refers to data being output from a single source. Reddy clearly teaches data being output from a single source such as the Look-up-Table 103 of Fig. 1 and Fig. 2 and then data are provided to the CRTs and LCDs. Moreover, Tjandrasuwita also suggests the claim limitation of "a single output that can provide data to both CRTs and LCDs" because Tjandrasuwita teaches in Fig. 1 a single output within the display graphics controller 107 with the same data being sent to the CRTs and LCDs from that single output within the graphics controller 107.

It is clear that Reddy teaches a graphics controller having a single output within the graphics controller that can provide data to both CRTs and LCDs and Tjandrasuwita teaches a graphics controller having outputs that can provide data to both CRTs and LCDs. Tjandrasuwita's graphics controller has a single data input and two data ouputs to the LCDs and CRTs. Tjandrasuwita's graphics controller processes the image data coming from the memory interface, formats the processed data, and passes the same data to the two output data lines, as can be seen in Figure 1. Therefore, there is a single output within the graphics controller of Tjandrasuwita. Moreover, Tjandrasuwita could have incorporated the Reddy's graphics controller to replace its own graphics controller to produce a single output that can provide data to both CRTs and LCDs to provide a single video controller which can control more than one video display having the SAME or COMMON resolution and refresh rate for diverse display devices (Reddy column 3). Although the internal structure of Tjandrasuwita is not described, it is clear from the internal structure of Reddy that Tjandrasuwita's graphics controller has a multitude of blocks similar to Reddy's wherein a single output exists before being separated into two different data paths to be routed to the CRTs and LCDs (See Reddy Figures 1-2 and Tjandrasuwita Fig. 1) to provide a single video controller which can control more than one video display having the same resolution and refresh rate (Reddy column 3).

3) Tjandrasuwita could have incorporated the video controller of Reddy within the Tjandrasuwita's integrated processing circuit 101 to provide a single output for the LCDs and CRTs because such a construction would have provided a means driving displays of different types from a single output (Reddy Figures 1 and 2; column 1-5) to provide a single video controller which can control more than one video display having the SAME IMAGE resolution and refresh rate (Reddy column 3). Moreover, Reddy further discloses a grayscale color lookup and a logic device 157 and 257 and attribute controller in the video controller to create image signals for the display devices and Tjandrasuwita teaches outputs from the display controller can be displayed in CRTs and LCDs (Tjandrasuwita Figure 1). Tjandrasuwita could have incorporated the video controller of Reddy to be attached to an output from Tjandrasuwita's integrated processing circuit 101 to provide a single output for the LCDs and CRTs. Such modification would have been required for portable computers or multimedia presentation for DISPLAYING the image having the SAME resolution and refresh rate ON BOTH the LCD and CRT DISPLAYS and SWITCHING IMAGES BETWEEN the LCDs and CRTs from the single output when desired (Reddy column 3).

Jeffery A. Brier

JEFFERY BRIER
PRIMARY EXAMINER